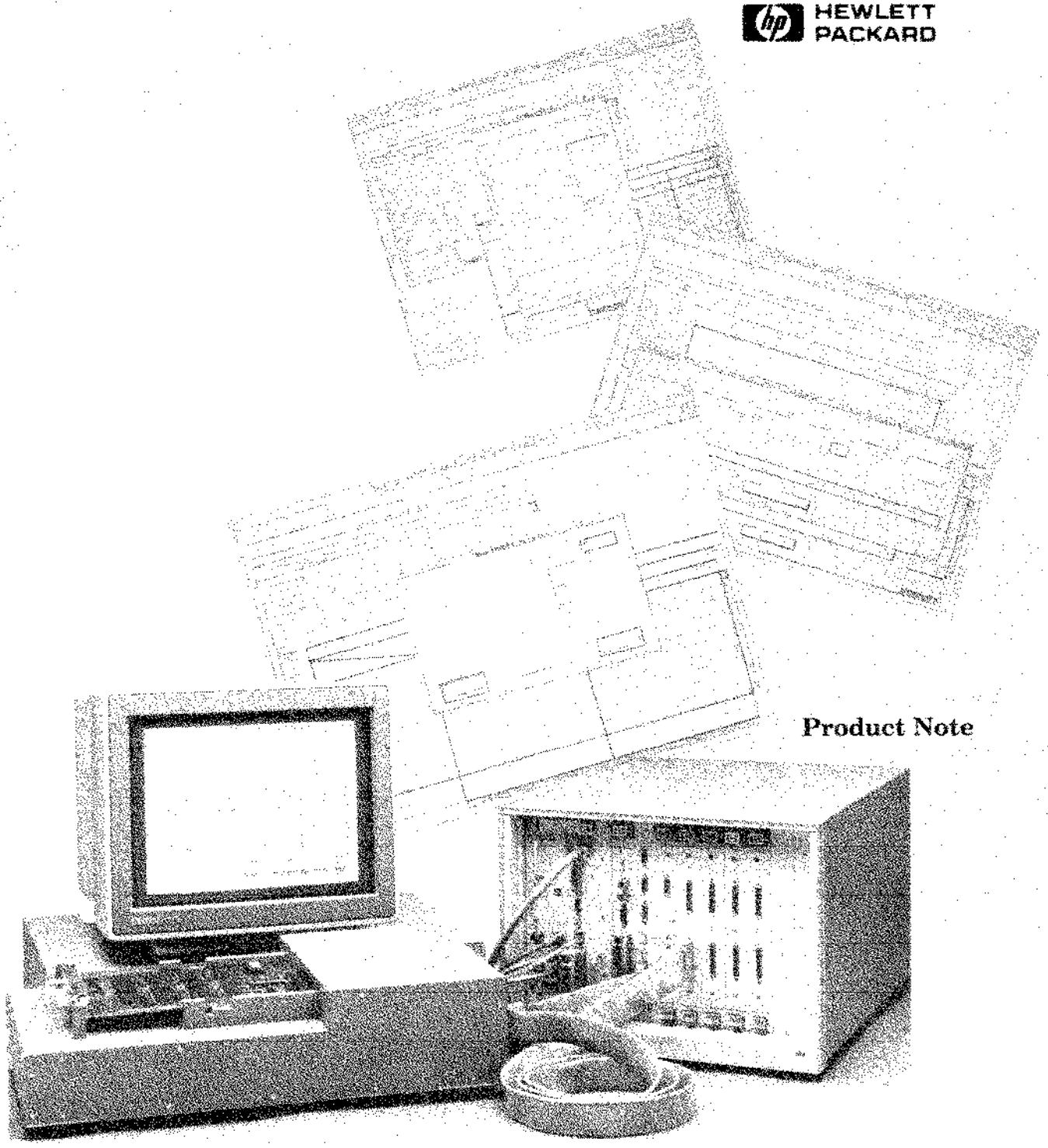
HEWLETT PACKARD



Product Note

HP 75000 Model D20
Digital Functional Test System

HP 75000 Model D20 Digital Functional Test System

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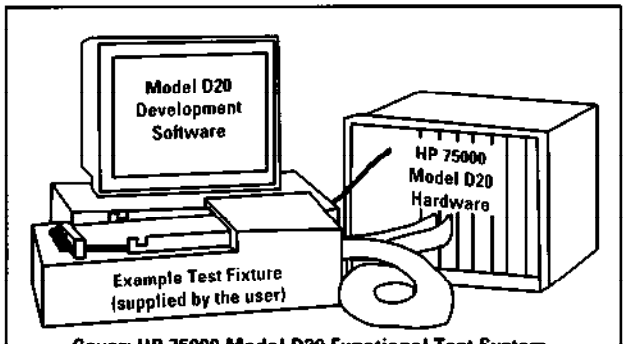


Cover: HP 75000 Model D20 Functional Test System shown does not include the test fixture.

Introduction

The HP 75000 Model D20 Digital Functional Test System is designed for functional testing of digital devices in manufacturing where high test throughput and low cost-per-channel are required. The Model D20 can test a wide variety of TTL and CMOS devices under test (DUTs), including modules and printed circuit cards containing digital bus architectures.These bus interface structures (Figure 1) typically have 8/16/24/32-bit addresses and data buses—and other lines including control, handshake, and clock. Some lines such as data, for example, are bi-directional, while others may be input or output.Test access is typically by edge connector.

The Model D20 Digital Functional Test System is intended for applications where high-quality digital stimulus/response tests are required and certain timing relationships must be maintained. The Model D20 emulates the signal patterns and timing to the DUT. It may be programmed to produce data patterns, control, handshake, and clock signals like those the DUT requires for normal operation. A typical DUT timing diagram is shown in Figure 2.

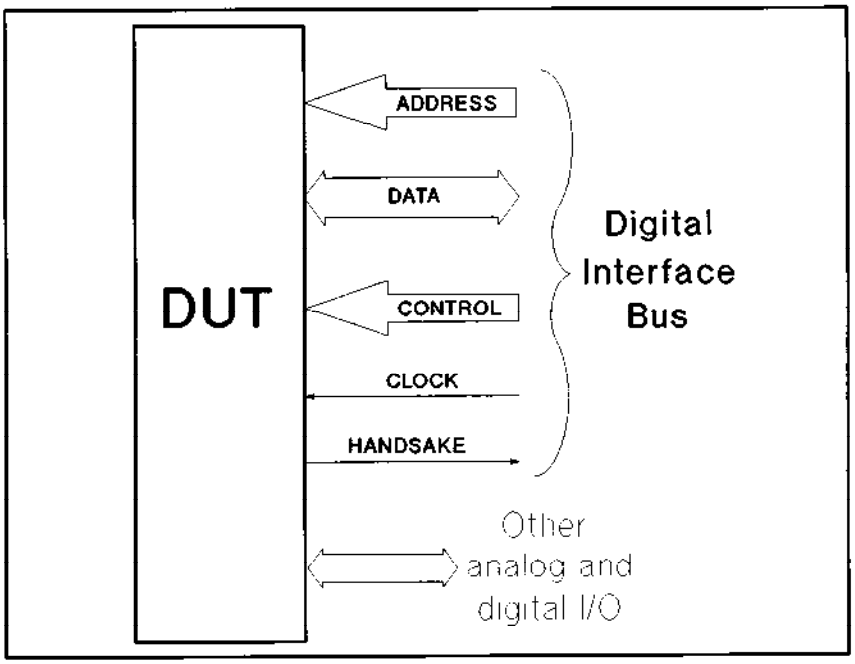


Figure 1.
DUT examples: Telecom line card, PC plug-in board, avionics module, workstation graphics board, plug-in modules for standard and proprietary modular instrument architectures.

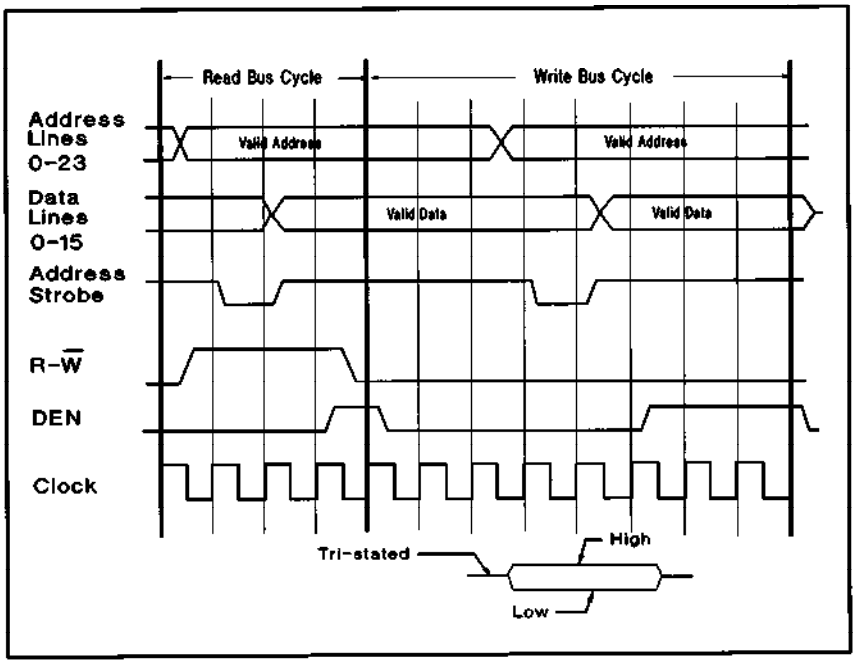
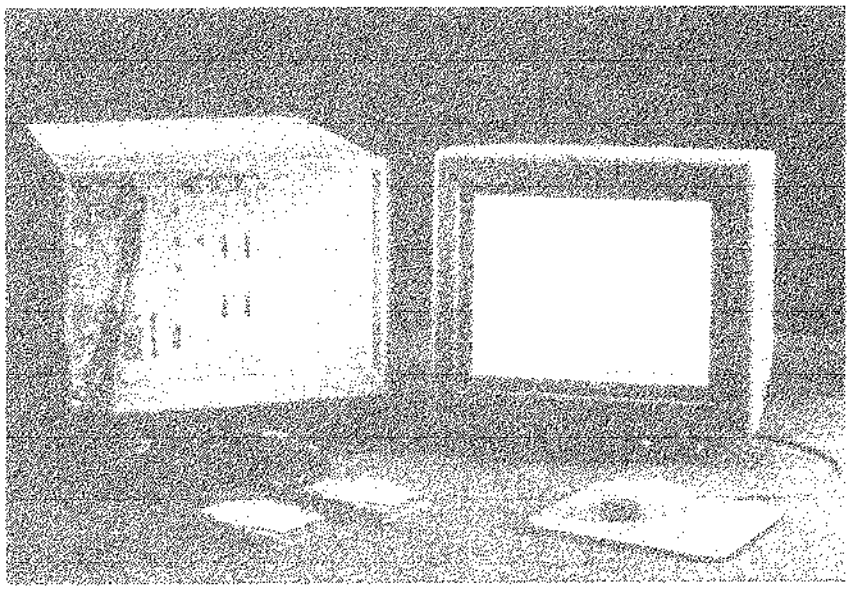


Figure2.
Typical DUT timing diagram

The Model D20 provides users a set of hardware and softeware tools with unequaled cost effectiveness. Its powerful development software can be utilized to quickly define the digital tests and create the test code. The Model D20 uses the latest industry standard architectures, thereby, protecting the user's test equipment investment. Some of the more important attributes and benefits of the Model D20 are summarized here.

- A *scaleable architecture* based on the VXIbus Standard means that the system can be configured to meet the performance needs today, but easily expanded to meet mixed signal functional test needs in the future. The VXIbus standard, an instrumentation extension of VMEbus, gives users a broad choice of VMEbus and VXIbus modular products and offers the best *protection against obsolescence.*
- A *standard command language* based on the new industry standard, *SCPI* (Standard Commands for Programmable Instruments), means that test software can be *hardware independent.* Software developed for the Model D20 today is preserved in the future when the test system is upgraded with performance enhanced Model D20 hardware.
- Active *pods extend the measurement accuracy* up to two meters from the front panel of the Model D20. Additional system accuracy is provided using the *automatic pin-to-pin de-skew* and *pod cable length compensation.*



HP 75000 Model D20

- Several features of the Model D20 *optimize test throughput. Deep segmentable memory* containing multiple tests allows the Model D20 to perform long uninterrupted test sequences without time consuming test pattern loads. Its *real-time compare* feature allows fast test execution. The Model D20's 20 MHz pattern and 40 MHz maximum timing clock rates allow most DUTs to be tested at full speed.
- The Model D20's *flexible timing features* allow it to test DUTs with complex timing cycles. Different timing cycles can be selected *'on-the-fly'* as the test progresses from vector to vector. It handles bus handshaking and wait states and includes comprehensive triggering for mixed-signal testing.
- The *development software* is based on *industry-standard X Windows System Version 11® and OSF/Motif®***. This mouse-driven graphical interface with pull-down menus allows users to quickly develop digital tests. The software can be used standalone to create timing cycles and to edit vector files. The Model D20 hardware also can be connected to the development workstation providing *on-line debugging* of the digital test.

** X Windows System and OSF/Motif are registered trademarks of the Massachusetts Institute of Technology and Open Software Foundation respectively.

The Hardware

The Model D20 consists of three major hardware components and development software (Figure 3):

- 160 MHz Timing Module (HP E1450)
- 20 MHz Pattern I/O Modules (HP E1451/E1452)
- Timing and Pattern Pods (HP E1453, HP E1454) (Figure 4)
- Digital Test Development Software (HP E1496)

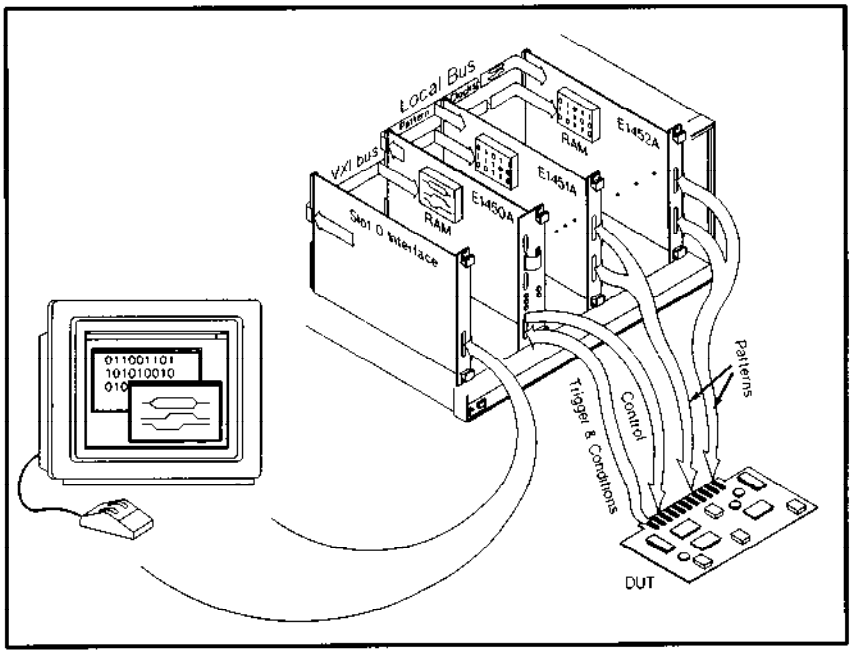


Figure 3. HP 75000 Model D20 Digital Functional Test System

HP E1450 160 MHz Timing Module and HP E1453 Timing Pod

The HP E1450 160 MHz Timing Module is a two-slot, C-size VXIbus register-based module containing a timebase, timing generators, trigger circuits, wait-for-condition circuits, end-if-ready circuits, marker circuits, and sequencer. These circuits supply cycle-by-cycle timing and control information to the other sections of the Model D20. Please refer to the block diagram in Appendix II.

The HP E1450 provides control signals for the DUT and timing for the sequence of patterns that are generated or recorded by the HP E1451/E1452 Pattern I/O modules. The timing module may be externally synchronized with signals from other instruments in the system or the DUT.

Emulation of complex bus cycles is made possible with up to 256 timing cycles. On-the-fly timing changes allow parameters such as cycle length and edge placement to change from cycle to cycle. Margin testing can be accomplished by varying timing edge placement. Edge placement resolution is 6.25 ns.

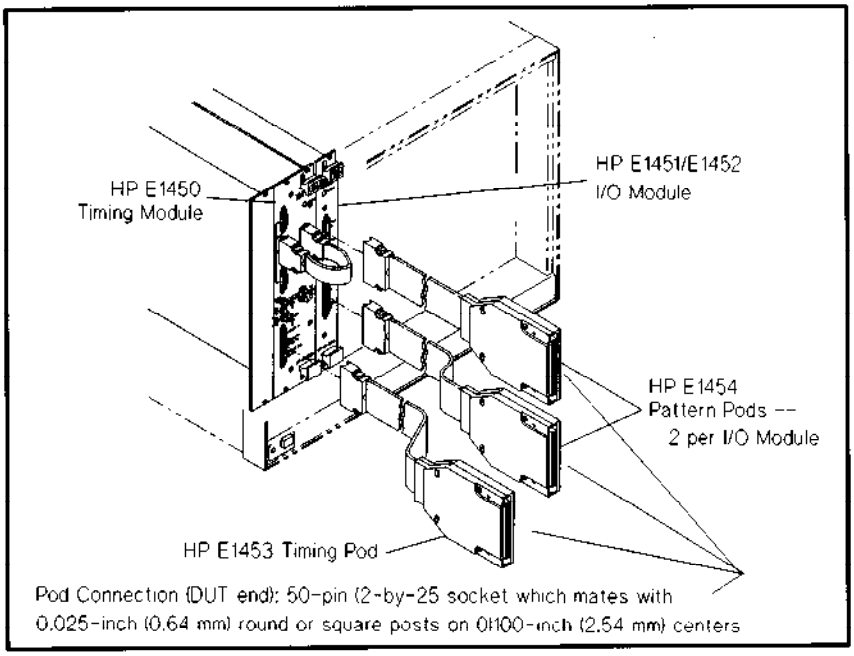
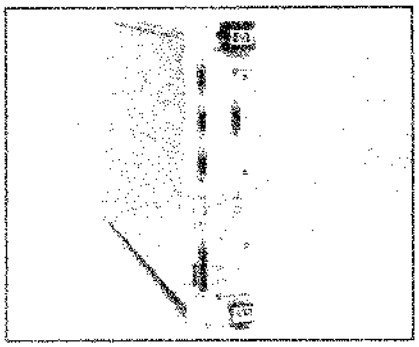
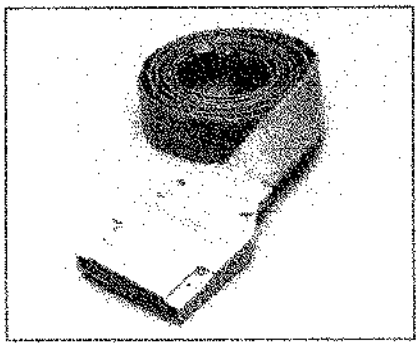


Figure 4. Timing and Pattern I/O Pods



HP E1450A Timing Module



HP E1453A Timing Pod

The HP E1450 provides 12 pattern clocks (six for stimulus, six for response) to as many as 10 HP E1451/E1452 Pattern I/O Modules in the same VXIbus mainframe (Figure 5). *Note: some power-limited VXIbus mainframes may not support a maximum of 10 pattern I/O modules.* The timing module also supplies up to eight general-purpose control signals for strobes, clocks, etc., to the DUT for synchronizing ports that must clock together.

The timing module can be externally synchronized with the DUT or other instrumentation. Triggers can be received from the VXIbus backplane, front panel SMB connectors, or the DUT. Ten qualifier input lines and three expression evaluators permit the system to wait for conditions (Boolean combinations of the 10 'Q' lines) within a test. An additional expression evaluator is provided for trigger qualification. Programmable marker outputs, available from SMB connectors on the front panel of the timing module and also over the VXIbus trigger bus lines, can be used to trigger other VXIbus or GP-IB instruments. Bus 'wait states' can be implemented with the end-if-ready function in conjunction with the Ready input.

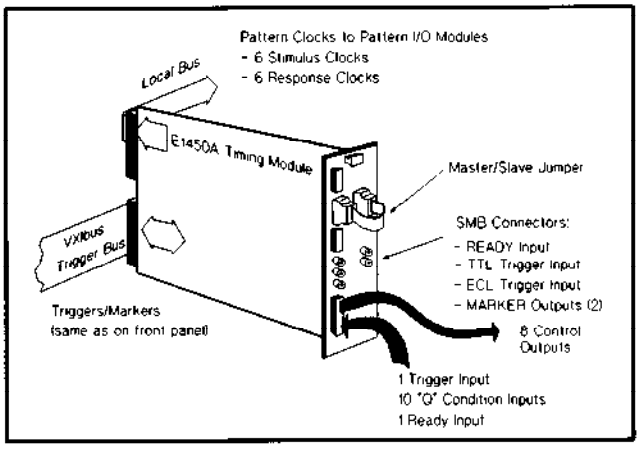


Figure 5. HP E1450 Timing Module

For large test systems exceeding the capacity of one VXIbus mainframe, a second or third mainframe may be connected using the HP E1482 VXIbus Extender. One HP E1450 Timing Module located in the root mainframe can act as a master for two additional HP E1450 slaves located in the extended mainframes. Control of a total of 30 Pattern I/O Modules (960 pins) is possible given that the mainframes can deliver sufficient power. Master/slave assignment is done by connecting a master/slave cable from a master connector on the master module to the slave connector on each of the slaves. See "Configuring and Ordering the Model D20" later in this document.

The HP E1453 Timing Pod (Figure 4) extends measurement accuracy to a DUT located up to two meters from the front panel of the Model D20. The pod is an active device which not only improves the Model D20's ability to drive DUT inputs, but also minimizes loading on DUT outputs. Signal delay in the cable is automatically compensated for by the Timing Module at power-on.

The Timing Pod buffers the eight control signals out to the DUT as well as the 10 'Q' lines, a ready line and a trigger line into the HP E1450 module. When the HP E1453 is not used, the Control and 'Q' lines can be accessed via the HP E1450's pod connector; trigger and ready lines are available on SMB connectors.The pod is supplied with a 2.1–meter cable. One pod per Timing Module is required.

Note: More detailed information about each of the inputs and outputs of the timing module is contained in the **Specifications** section of this document.

HP E1451/E1452 20 MHz Pattern I/O Modules and HP E1454 I/O Pod

The HP E1451 Pattern I/O Module and HP E1452 Terminating Pattern I/O Module (Figure 6) are single slot C-size VXIbus register-based modules. They are used to send or receive pattern data from the DUT. Each I/O module contains four identical 8-pin ports (32 I/O pins). Each port can be independently programmed to either output (stimulus), record (response), or real-time compare. Bi-directional I/O is created by connecting the I/O pins of two or more ports together. For example, an eight-pin bi-directional I/O is made by connecting one 8-pin port to a second 8-pin port with one port defined as the stimulus port and the other as the response port. The stimulus port is then tri-stated when the response port is active. A signal supplied by the timing module or from an external source is used to tri-state a port's I/O pins.

Test throughput is maximized by programming the I/O pins to perform real-time comparison of response patterns. Deep memory (64 Kbits) dedicated to each pin holds test patterns and records response pattern data. This memory is segmentable so that it can be used for one large test or split into multiple tests. This minimizes the need to load new patterns.

The HP E1451 and HP E1452 are identical except that the HP E1451 passes along the Local Bus pattern clocks to the next module whereas the HP E1452 terminates the pattern clock lines. The HP E1452 Terminating Pattern I/O Module must be the last module of the Pattern I/O module set so the Local Bus is properly terminated when the HP E1450 Timing Module is used. If external timing is used in lieu of the timing module, then only HP E1451 Pattern I/O modules are required.

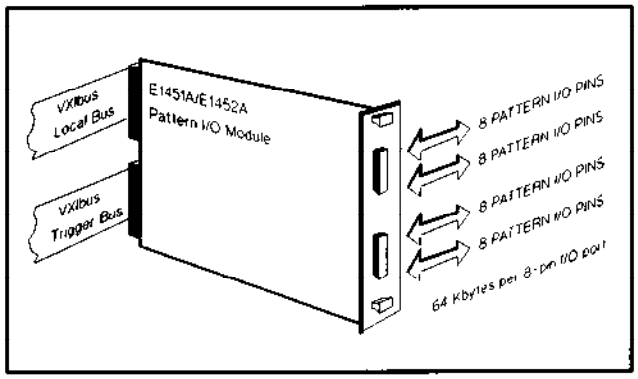
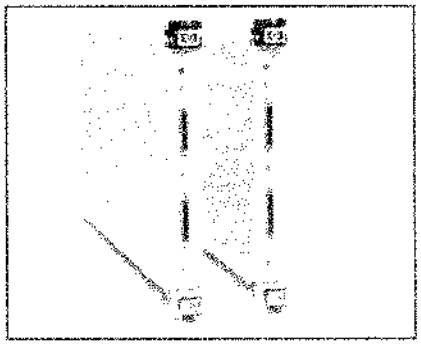
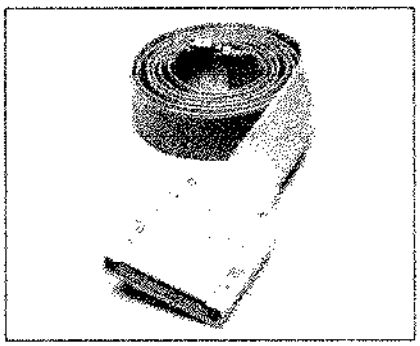


Figure 6. Pattern I/O Module

The HP E1454 Pattern I/O Pod (Figure 4) extends measurement accuracy to a DUT located up to two meters from the front panel of the Model D20. Each pod buffers the input and output signals for two of the four HP E1451/E1452 I/O ports; two pods are required for each pattern I/O module[1] . This improves the Model D20's ability to drive DUT inputs and minimize loading on DUT outputs. Response pattern clocks are delayed on the Timing Module so that timing is correct at the DUT. And pin-to-pin skew on the pattern I/O lines is compensated for, resulting in a system that is always within specifications. The pattern I/O pods also provide inputs for tri-state control and external clock. The HP E1454 is supplied with a 2.1–meter cable.



HP E1451A/E1452A Pattern I/O Modules



HP E1454A Pattern I/O Pod

[1] If pods are used on any port or the timing module, then there must be pods on all ports and the timing module.

The Software

The purpose of the E1496A development system software is to enable the user to quickly and easily take advantage of the HP75000 Model D20 hardware. The development system software provides a graphical, menu-driven environment. It runs on HP-UX*, and is based on the X Windows System® and OSF/Motif ®. It gives the user direct control over what the system is doing, without having to translate every detail into a command of some sort. Timing is specified graphically, just as a timing diagram might appear in a data book. Data is separated from timing, and is entered into what is essentially a simple spreadsheet. This allows the user to think in terms of the task to be performed, not in terms of commands to an instrument.

The E1496A development system software can be used without the Model D20 hardware to develop tests. But, once the hardware is added, comprehensive debug becomes available. Also, although the software can run the HP75000 Model D20 directly, the user will typically have the development system software produce an output file that can be taken to the test system and incorporated with whatever test executive software the user has chosen. With this structure, it does not matter what type of software or computer the user has in the test stand; the E1496A can always be used to develop the digital test for the HP75000 Model D20.

* HP-UX is Hewlett-Packard's implementation of the UNIX (R) operating system. UNIX is a registered trademark of AT&T in the U.S.A. and other countries.

Figure 7 gives an overview of how the software works. The object of the software is to let the user program the system in the same way that the DUT (device under test) works. The software is divided into two major windows, the Pattern Sequence Spreadsheet and the Timing Cycle Spreadsheet. Both spreadsheets have time on the horizontal axis and pin group names down the vertical axis.

The DUT's timing cycles are programmed graphically using the Timing Cycle Spreadsheet.

The data patterns are entered into the Pattern Sequence Spreadsheet. Also note that each vector is made up of data patterns and a timing cycle name. These two spreadsheets work together to let the user program the hardware in a way that is very easy to understand.

The software provides many different windows, menus, and dialog boxes to help the user develop tests. The major steps will now be described in more detail.

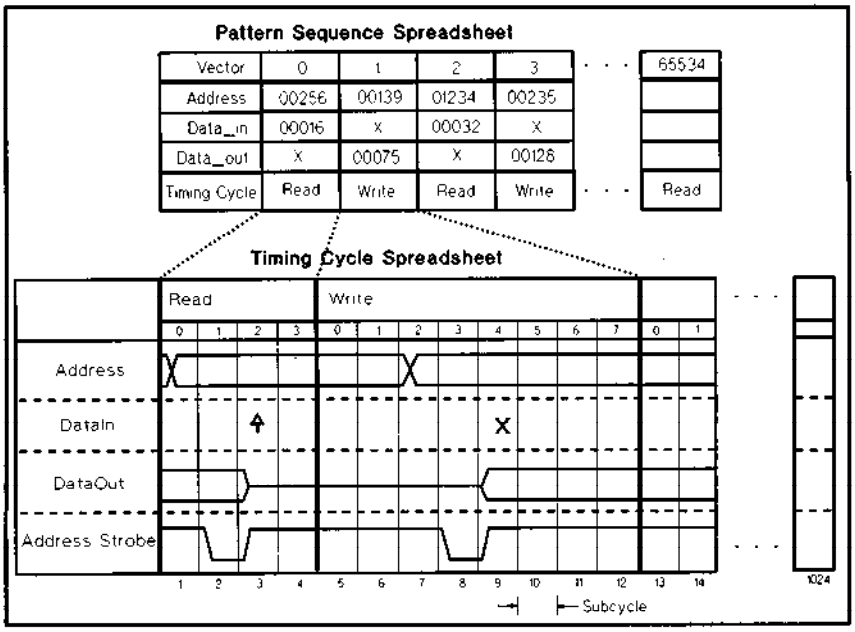
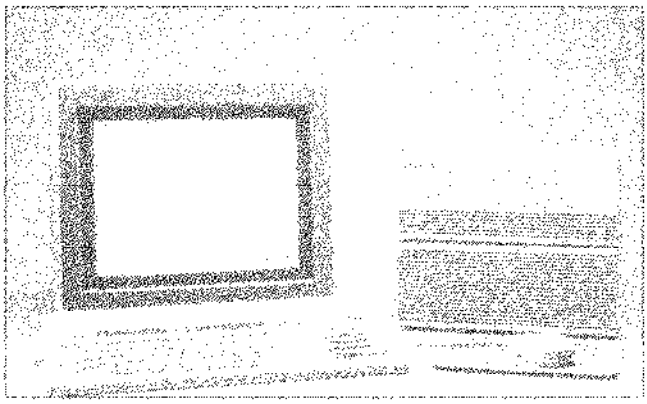


Figure 7. The HP E1496A allows the developer to easily specify vectors with desired pattern sequence information and timing cycles for the DUT.



HP E1496A Digital Test Development Software

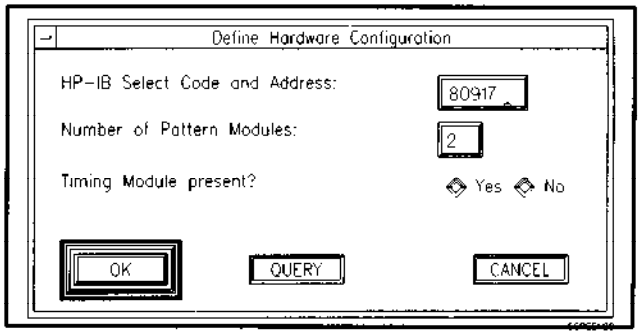


Figure 8. Hardware Configuration filled out with timing module and two pattern I/O modules.

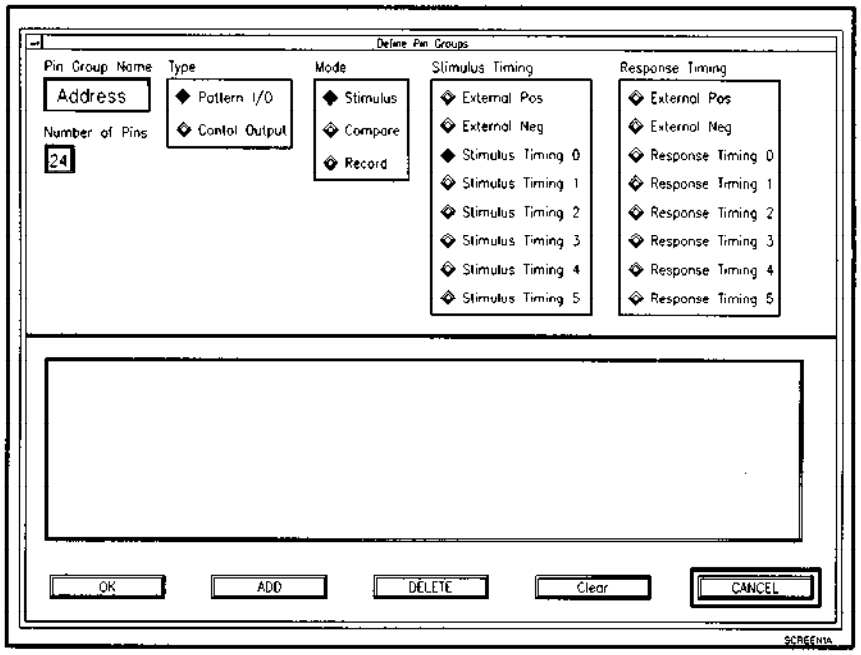


Figure 9. Define Pin Groups menu with some definitions complete.

Specify the Hardware Configuration

The first step is to tell the software what hardware configuration is to be used during actual testing of real devices. Tests can be developed without the D20 hardware, but the user must specify which hardware will ultimately be used. The Define Hardware Configuration dialog box (Figure 8) is used for this purpose.

After the HP-IB address is entered, the 'Query' button causes the software to communicate with the hardware at the specified HP-IB address. If a HP75000 Model D20 is found, the 'Number of Pattern Modules' field and 'Timing Module present?' will be set to represent the hardware found in that system.

Define the DUT Signal Names

The Define Pin Group Names dialog box allows the user to program using the DUT signal names such as "Address", instead of terms of the D20 hardware (such as "Slot 4, Port 1"). Here, the user enters the DUT signal names, signal type (pattern I/O or control), pattern I/O mode, and number of pins. This dialog box allows the user to select the timing of a given pin group by specifying external timing or one of the internal timing channels (the Timing Module has 12 timing channels (pattern clocks), six for stimulus and six for response). Figure 9 shows this dialog box partly filled in for the typical DUT found in figure 1. This dialog box can be called up later during development to edit or delete pin groups, or to add new pin groups.

Defining Timing Cycles

The Timing Cycle Spreadsheet (Figure 10) allows the user to enter DUT timing information graphically. The user defines timing cycles and each timing cycle specifies the duration of each vector and the timing for each signal. A timing cycle is made up of subcycles (each subcycle represents a period of time set by the system timing resolution).

The timing information is entered onto the Timing Cycle Spreadsheet by selecting a cell, and then specifying the event to go into that cell. The cell is selected by clicking at the intersection of the 'Pin Group Name' row for which the timing event is desired, and the subcycle column in which the event is to take place. The event is then entered into the cell by selecting it from the Timing Cell Values menu (Appendix I).

There are three things to note here. First, timing cycles can be of different lengths. Second, the same Pin Group Name can change state at different times in different timing cycles. For example, note that "Address" changes data in subcycle zero in timing cycle "Read", and in subcycle two in timing cycle "Write". Third, different pin group names can change state at different times in the same timing cycle. For example, note that "Address" changes data in subcycle zero in timing cycle "Read", and "DataOut" changes data in subcycle two of the same timing cycle. Each vector in the Pattern Sequence Spreadsheet can refer to any of the defined timing cycles, switching between them with no pause in the test. This is referred to as changing timing "on-the-fly."

Defining Pattern Data

The Pattern Sequence Spreadsheet (Figure 11) allows the user to define the test vectors.

The pattern type pin group names are on the left, one per row. Across the top are vector numbers, one per column. Each vector is made up of a pattern value for each pattern type pin group, and the name of a timing cycle from the Timing Cycle Spreadsheet. The timing cycles defined in the Timing Cycle Spreadsheet specify when the pattern ports clock data, the Pattern Sequence Spreadsheet defines that data.

Each vector is linked to a timing cycle. In the row on the Pattern Sequence Spreadsheet labeled 'Timing Cycle', the user enters in the name of the timing cycle to be used for applying that vector ("Read", "Write", for example). The timing cycle determines the duration of the vector, and when each pin group will have its data output or received. Typically there are a small number of different cycles a particular DUT uses.

Pattern data is entered into this spreadsheet by the test developer. If a timing cycle name is specified for the vector, and that timing cycle has specified that a pin group should be three-state or don't care, then the corresponding cell on the Pattern Sequence Spreadsheet is automatically filled with an X, to show that no data needs to be entered for that cell. Data can also be specified as three-state by entering an "X" into the cell. For pin groups of more than one pin, the pin group can be expanded into one row per bit, allowing the values to be viewed and edited as binary digits. ASCII data files can also be brought into the Pattern Spreadsheet. This will be covered in more detail later.

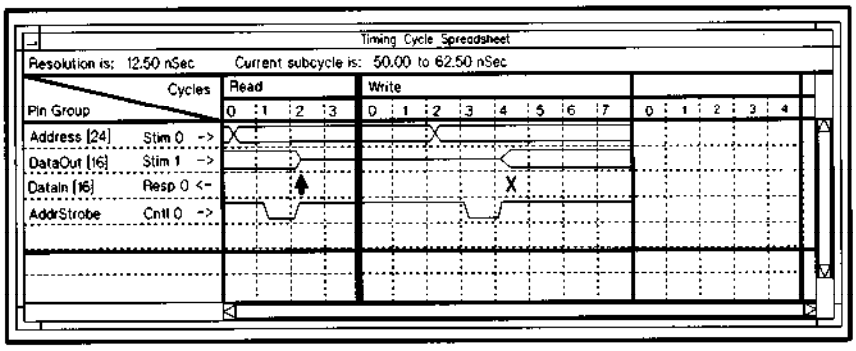


Figure 10.
Timing Cycle Spreadsheet

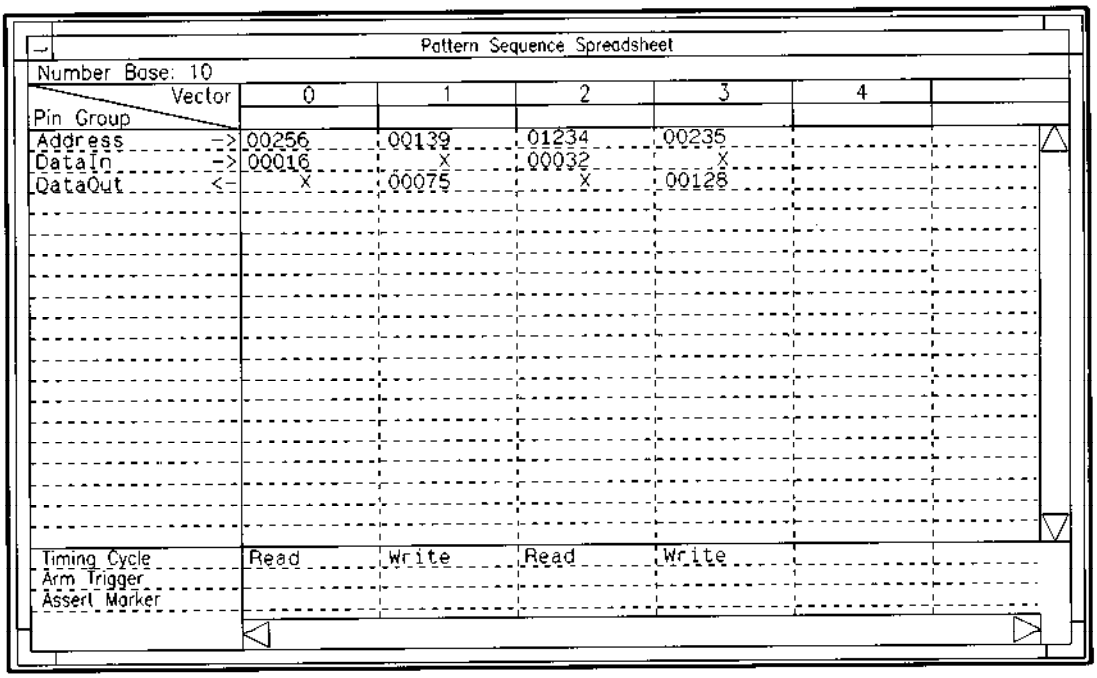


Figure 11. Pattern Sequence Spreadsheet with four (4) vectors filled in.

Debugging the Test

When the development system is connected directly to the Model D20 hardware, extensive debug capabilities become available. There are two parts to debugging the digital test. First, the 'Rules Check' does a comprehensive check on the test defined. This check automatically ensures that the test violates none of the constraints of the hardware.

Second, the developer may run the defined test directly on the HP75000 Model D20 hardware; this is accomplished by using the 'Run Test' dialog box (Figure 12) selected from the Debug Menu (Appendix I). The test can run from start to finish, or single-stepped, either from the start of the test or from a breakpoint set in the Pattern Sequence Spreadsheet. While running the test, pin groups that are programmed to record data will read data back from the hardware and display it on the Pattern Sequence Spreadsheet when the test stops or pauses. If a comparison error is detected by the hardware, the Pattern Sequence Spreadsheet will update and display the vector that failed. For each pin group that detects a failure, the actual received data is displayed along with the expected result and the pin group mask. The pin group mask value can be specified for each pin group programmed to compare data, and masks off individual bits from the comparison.

Direct I/O allows the user to bypass execution of the test and directly communicate with the Model D20 hardware. The user can force values on Stimulus mode Pattern I/O pins and Control Outputs. The current value of a Compare or Record mode Pattern I/O pins can be read, as can the state of the Boolean expression for the three conditional tests or for the trigger qualifier. The control output pins can be forced into or out of three-state, and a trigger can be forced as well.

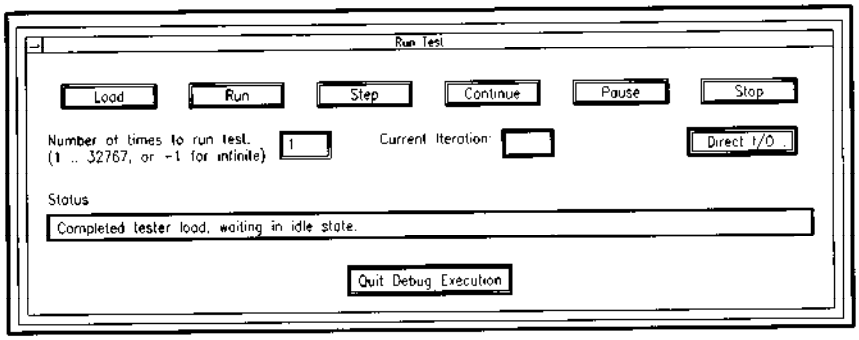


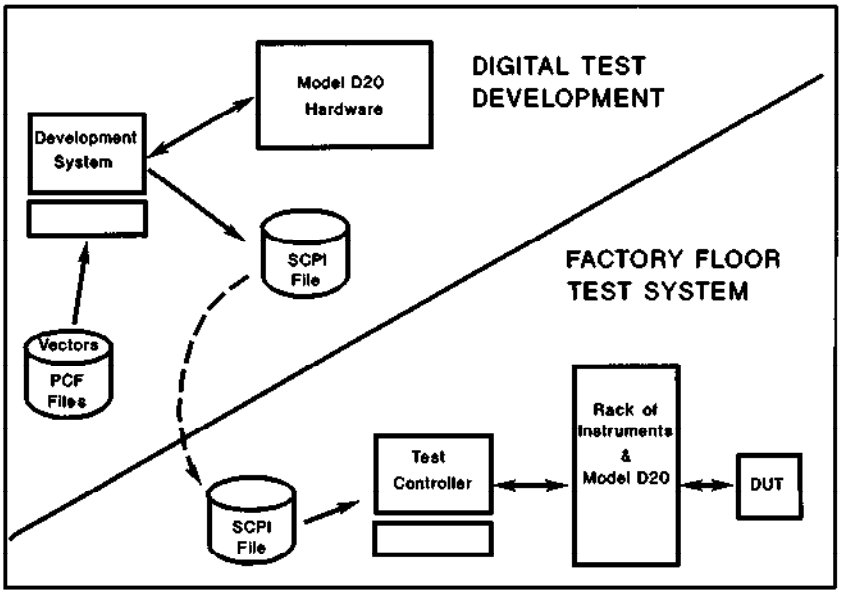
Figure 12. Run Test dialog box.

File Operations

For users who generate vectors with a program or with a simulator, the development system software can import files in the Pattern Capture Format (PCF)*. If the user produces vectors in the PCF format, or translates simulator output to the PCF format, the system will import that file into the Pattern Sequence Spreadsheet. The vectors will be filled in with the pin group values and the timing cycle names. The user then defines the timing cycles using the Timing Cycle Spreadsheet.

The user may wish to create a test as a number of short tests, each one for perhaps a different subsection of the DUT. Each test is written and debugged, and then all brought together to form one test. This is easily accomplished with the development system software using the 'File Combine' feature. Here, the system takes the already loaded test, and merges it with a test stored in a file to produce one combined test.

Finally, the user stores the completed test as an ASCII file. This file, consisting of SCPI (Standard Commands For Programmable Instruments) commands, can be taken to the test system and incorporated with whatever test executive software the user has chosen. With this structure the test software and controller used in the test stand are independent of the development environment.



* PCF is an ASCII file format designed by the Manufacturing Test Division of Hewlett-Packard.

Mixed Signal Testing

Many devices that need to be tested have both digital and analog signals. The HP75000 Model D20 is designed to integrate into a mixed signal test, as well as to do digital only tests. One important aspect of creating a mixed signal test is the ability to coordinate with other instruments by the use of triggers. For example, to test a digital to analog converter, the HP75000 Model D20 can be programmed to apply some number of vectors, trigger another instrument, such as a voltmeter, and then wait for a trigger back from that instrument before continuing with more digital vectors. This can be done without any intervention from the test system controller, keeping the test running at the best possible speed.

On the Pattern Sequence Spreadsheet (Figure 11), there are two rows labeled 'Arm Trigger' and 'Assert Marker'. These rows allow the user to coordinate the test with other instrumentation. Arming a trigger causes the D20 to pause before executing that vector, and then continue after the trigger is received. Input triggers can come into the timing module, either to the pod, if present, or to a front panel connector. Any of the VXI trigger bus lines can be selected as well. The trigger can be qualified using the condition inputs. If the trigger qualifier is enabled, the qualifier expression must evaluate to True for a trigger to be accepted.

Enabling the 'Assert Marker' row within a vector causes the D20 to produce an output trigger pulse. This Marker always comes out the timing module front panel connectors. It can also be routed to any of the VXI trigger bus lines. This use of both the VXI trigger bus lines as well as front panel and pod connections for triggering allows the HP75000 Model D20 to take advantage of VXI features while also allowing it to be integrated with traditional rackand-stack instrumentation.

Handshaking with the Device Under Test

Synchronous and asynchronous type buses both typically use some kind of handshaking protocol for indicating when they need more time, and when they can continue. Asynchronous busses typically have control lines which tell the DUT when there is data for it, and other control lines for it to indicate when it is ready to proceed. For the control lines to the DUT, pin group names can be defined as control output lines from the timing module and desired signals specified within each timing cycle. For the control lines from the DUT, there are three test conditionals that can be defined for use within the timing cycles. Each conditional test is defined as a Boolean logical expression that uses the ten timing module 'Q' input lines as variables, just like the trigger qualifier.

The Timing Cycle Spreadsheet in Figure 13 shows a conditional test which is enabled (Cond 0).

This condition will cause the test to execute until a vector specifies this timing cycle. The timing cycle will then proceed until the subcycle containing the 'Yes' is encountered. The tester will then stop after that subcycle until the result of the Boolean expression becomes true. For asynchronous devices, the control outputs from the timing module produces one side of the handshake, with the 'Q' input lines and the conditional tests waiting for the completion of the handshake.

Synchronous DUTs typically work in a different fashion. If the DUT is not ready to proceed, it will change the state of a control line to indicate that it is not ready. This is sampled during the cycle, and if not ready, a 'wait-state' is inserted into the cycle. The Ready input to the timing module will then be sampled. If it is true, the timing cycle ends and the test continues with the next vector from the Pattern Sequence Spreadsheet. If the line is not true, the timing cycle continues to execute subcycles. Multiple wait states per cycle can be programmed (up to the maximum number of subcycles available).

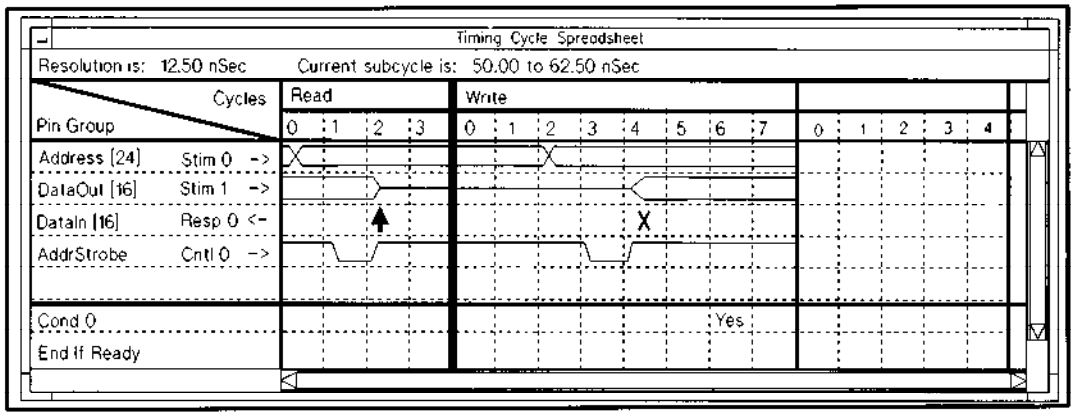


Figure 13. Timing Cycle Spreadsheet with Cond 0 and End If Ready at the bottom.

Specifications

System Skew And Accuracy

The time interval from the beginning of a sequence to the following events is as given:

- To a high-to-low or low-to-high transition on any pattern stimulus pin:

  (1+TBE)(PROGRAMMED VALUE) ± 3.0 nSec (with or without pods)

- To a high-to-low or low-to-high transition on any control output pin:

  (1+TBE)(PROGRAMMED VALUE) ± 3.0 nSec (with or without pods)

- To the actual sampling instant of any pattern response pin:

  (1+TBE)(PROGRAMMED VALUE) ± 3.0 nSec (with or without pods)

- To any pattern stimulus pin entering tri-state:

  1.4 nSec + (1+TBE)(PROGRAMMED VALUE) ± 5.4 nSec (with pods)
  7.7 nSec + (1+TBE)(PROGRAMMED VALUE) ± 4.4 nSec (without pods)

- To any pattern stimulus pin exiting tri–state:

  –1.4 nSec + (1+TBE)(PROGRAMMED VALUE) ± 6.7 nSec (with pods)
  5.2 nSec + (1+TBE)(PROGRAMMED VALUE) ± 5.2 nSec (without pods)

NOTE: In the foregoing, TBE is timebase error which is the same for all events and specified to be within ± 0.01%. PROGRAMMED VALUE is the sum of the programmed durations of all preceding cycles in the sequence plus the programmed delay from the beginning of the current cycle to the event in question.

These specifications apply for the following conditions:

- Stimulus pattern and control pins loaded with 50 pF and 500 Ω to ground
- Any sequence of cycles and event placements within those cycles
- Any sequence length
- Any stimulus or response data values
- Systems comprised of up to three HP E1400 mainframes
- Any ambient temperature between 0 and 55 °C Up to three years from last calibration

Stimulus transitions are measured at 2.5 V; response thresholds are 1.5 V.

When Waiting-for-Trigger and/or Waiting-for-Condition states are encountered, time intervals will be increased by the length of time spent in those states. **(See Trigger Specifications And Wait-for-condition Specifications.)**

NOTE: The above specifications guarantee that any two events (except entering or exiting tri-state) programmed to be simultaneous will occur within 6.0 nSec of each other.

HP E1450 160 MHz Timing Module And HP E1453 Timing Pod

Sequencer Specifications

Memory Depth 65,536 (64 KB) bytes.
Multiple test sequences may co-reside in memory.

Functions
Timing Cycle Selection, Stopping Point, Breakpoints, Markers, and Trigger Arming, all programmable on a cycle-by-cycle basis.

Timebase Specifications

Timing Cycle Duration

Minimum:	50 nSec or 4 Subcycles, whichever is greater
Maximum:	1024 Subcycles (see **Number Of Timing Cycles** below)
Resolution:	One Subcycle

Subcycle Period

Minimum:	6.25 nSec
Maximum:	409.6 µSec
Resolution:	6.25 nSec
Accuracy:	0.01%

Number Of Timing Cycles
Up to 256. The total length of all Timing Cycles may not exceed 1024 Subcycles.

Stimulus Timing Generator Specifications

Function
Provides six Stimulus Pattern Clock signals which define edge placements for HP E1451A/52A Pattern I/O Ports configured in Stimulus mode. (Each I/O Port is programmed to use one Pattern Clock as its timing reference.) Pattern Clocks are independent of each other and may have different delays in different Timing Cycles.

Stimulus Pattern Clock Delay
(from beginning of Timing Cycle)

Minimum:	0 Subcycles
Maximum:	Timing Cycle Duration – 1 Subcycle
Resolution:	1 Subcycle
Miscellaneous:	No sequence of Timing Cycles may be allowed to cause Pattern Clocks to occur less than 50 nSec apart.

Response Timing Generator Specifications

Function
Provides six Response Pattern Clock signals which define sampling points for HP E1451 /52 Pattern I/O Ports configured in Response mode. (Each I/O Port is programmed to use one Pattern Clock as its timing reference.)Pattern Clocks are independent of each other and may have different delays in different Timing Cycles. If the HP E1453 Pod is used, the Response Timing Generator is automatically delayed from the Stimulus Timing Generator by an amount equal to the pod's round-trip delay. The timing frame-of-reference is thus moved to the location of the DUT, up to 2.1 meters from the mainframe.

Response Pattern Clock Delay
(from beginning of Timing Cycle)

Minimum:	0 Subcycles
Maximum:	Timing Cycle Duration – 1 Subcycle
Resolution:	1 Subcycle
Miscellaneous:	Each Timing Cycle must have exactly one Pattern Clock; no sequence of Timing Cycles may cause Pattern Clocks to occur less than 50 nSec apart.

Control Timing Generator Specifications

Function
Provides 8 general-purpose Control Signals to the DUT via the front-panel pod connector (or HP E1453 Pod, if present). Control waveforms can have multiple transitions in each cycle, and may differ from cycle to cycle. These outputs can be set directly and enabled or tri-stated programmatically. The Control Timing Generator is automatically delayed from the Stimulus Timing Generator to compensate for delays through the backplane and HP E1451/52 Pattern I/O Ports (and differences in pod delays, if pods are used in the system). This minimizes skew between Pattern and Control outputs.

Control Signal Edge Timing
Minimum Delay
(from beginning of Timing Cycle):
0 Subcycles
Maximum Delay: Timing Cycle Duration – 1 Subcycle

Resolution: 1 Subcycle

Minimum Programmable Pulse Width (high or low): 12.5 nSec
Skew:
Control to Control or HP E1451/E1452 output: 6 nSec, maximum*
Control to Control, same HP E1450: 3 nSec, typical

Risetime: < 5 nSec, typical

Falltime: < 5 nSec, typical

*** Specification assumes all Master/Slave cables are the same length.**

Ouput Levels
HP E1450A Module Outputs
Maximum Continuous Output Current: ± 24 mA per line
High, Open-Circuit: 4.4 V, minimum
Low, Open-Circuit: 0.1 V, maximum
Output Impedance: 50 Ω, typical
Capacitance
(outputs disabled): < 20 pF, typical

HP E1453 Pod Outputs
Maximum Continuous Output Current: ± 24 mA per line
High, Open-Circuit: 4.3 V, minimum
High, Sourcing 24 mA: 3.7 V, minimum
Low, Open-Circuit: 0.1 V, maximum
Low, Sinking 24 mA: 0.44 V, maximum
Capacitance
(outputs disabled): < 15 pF, typical

Trigger Specifications

Function
The Sequencer can be programmed to Arm the Trigger system at the beginning of any Timing Cycle. When this occurs, the system enters the Waiting-for-Trigger state and all Timing Generators stop. Once a trigger is received from the selected source and delayed by a programmable amount, the Timing Generators resume operation. If the delay for a certain trigger event expires before the system is in the Waiting-for-Trigger state, then that trigger will have no effect. If a second trigger is received before the delay for a previous trigger has expired, the second trigger will have no effect.

Trigger Sources
Eight VXI TTL trigger busses, two VXI ECL trigger busses, TTL- and ECL-compatible front-panel coaxial connectors (SMB-type), and a TTL-compatible input on HP E1453 Pod (if present). There is also an 'Immediate' source which has the effect of triggering the system immediately upon entering the Waiting-for-Trigger state. Finally, the system can be triggered programmatically, regardless of the selected source.

Trigger Slopes
The VXI ECL and TTL inputs are sensitive to rising and falling edges, respectively. Coaxial and Pod inputs can be programmed to be sensitive to rising or falling edges. There is no slope associated with the 'Immediate' source.

Trigger Qualification
Triggers from any source but 'Immediate' can be qualified by a user-defined Boolean expression ("CONDition3") of the ten 'Q' inputs. (Refer to WAIT-FOR-CONDITION SPECIFICATIONS below for details of how this expression is defined.) When the 'Q' inputs are in a state which makes the expression true, triggers are recognized; when the expression is false, triggers have no effect. This function can be programmatically disabled, resulting in unqualified triggering. Triggers from the 'Immediate' source are always unqualified.

Programmable Trigger Delay
The latency time of any trigger source but 'Immediate' can be programmatically increased by 0 to 409.59375 uSec in steps of 6.25 nSec.
(See **Trigger Timing** below for un-delayed latency times.)

Trigger Input Levels and Loading
Note: VXIbus TTL and ECL inputs meet VXIbus specifications

Front-panel TTL coaxial
High: > 2.0 V (internal 50 KΩ pull-up)
Low: < 0.8 V at < 250 uA
Capacitance: < 10 pF, typical

Front-panel ECL coaxial
High: ≥ 1.07 V at < 150 uA
Low: ≤ 1.48 V at ~ 1.5 uA
(internal 50 KΩ pull-down)
Capacitance: < 10 pF, typical

Pod TTL input
High: > 2.0 V (internal 50 KΩ pull-up)
Low: < 0.8 V at < 3.35 mA
Capacitance: < 10 pF, typical

Trigger Timing

Minimum Pulse Width (High or Low)
Note: VXIbus TTL and ECL inputs meet VXIbus specifications
Front-panel TTL: 6 nSec
Front-panel ECL: 4 nSec
Pod TTL input: 6 nSec
Minimum Time Between Triggers:
12.5 nSec + Programmed Trigger Delay
Latency Time:
Defined as the time which elapses from a (qualified) trigger from the specified source to the specified Control outputs, with Trigger Delay programmed to 0. Latency from the 'Immediate' source is 0; others are given by the table below. Latency times in the table consist of fixed delays which vary from unit to unit plus 6.3 nSec non-cumulative jitter.

Trigger Source	VXI TTL	VXI ECL	Coax TTL	Coax ECL	Pod TTL
To E1450 Outputs					
(minimum)	79 nS	75 nS	76 nS	74 nS	n/a
(maximum)	93 nS	87 nS	88 nS	86 nS	n/a
To E1453 Outputs					
(minimum)	99 nS	95 nS	96 nS	94 nS	106 nS
(maximum)	113 nS	107 nS	108 nS	106 nS	119 nS

Trigger Qualifier Timing

Setup time is defined as how long the 'Q' inputs must be stable before trigger edge from the specified source. Hold time is defined as how long the 'Q' inputs must remain stable after a trigger edge from the specified source.

Trigger Source	VXI TTL	VXI ECL	F-P TTL	F-P ECL	Pod TTL
E1450 'Q' Inputs					
(setup)	3 nS	7 nS	6 nS	8 nS	n/a
(hold)	**9 nS**	**3 nS**	**4 nS**	**2 nS**	**n/a**
E1453 'Q' Inputs					
(setup)	20 nS	24 nS	24 nS	25 nS	12 nS
(hold)	**-3 nS**	**-9 nS**	**-8 nS**	**-10 nS**	**2 nS**

Note: F-P means Front Panel

Wait-for-condition Specifications

Function

The HP E1450 contains four Expression Evaluators which continually evaluate user-defined Boolean expressions whose variables are the states of the ten 'Q' input lines. One evaluator, named 'CONDition3', produces the trigger qualifier (see **Trigger Specifications** above); the other three, named 'CONDition0', 'CONDition1 ', and 'CONDition2', are available for general synchronization and handshaking. The HP E1450's Timing Generators can be programmed to test any combination (including none) of CONDition0 through CONDition2 at the end of any Subcycle of any Timing Cycle. If any of the tested Conditions is false, the system enters the Waiting-for-Condition state and the Timing Generators stop. Operation resumes once all tested conditions become true.

Accepted Expression Elements

Variables:	'Q0', 'Q1', ... , and 'Q9', corresponding to the ten 'Q' inputs
Operators:	'AND', 'OR', 'EXOR', and 'NOT'
Constants:	'T' (for True) and 'F' (for False)
Parentheses:	'(' and ')' to bound expressions and indicate evaluation order

'Q' Input Levels And Loading

HP E1450 Module Inputs
High: > 2.0 V (internal pull-up)
Low: < 0.8 V at < 250 uA
Capacitance: < 10 pF, typical

HP E1453 Pod Inputs
High: > 2.0 V (internal pull-up)
Low: < 0.8 V at < 150 uA
Capacitance: <1 0 pF, typical

'Q' Input Timing

The following definitions apply to a Condition which is tested in a certain Subcycle:
Setup time is how long the 'Q' lines (at the specified input) must satisfy the condition before the end of that Subcycle (as observed at the specified output). Hold time is how long the condition must remain satisfied after that Subcycle. If the system is in the Waiting-for-Condition state, latency time is how long it takes to resume operation once all Conditions are satisfied. Latency time consists of a fixed delay which varies from unit to unit plus 6.3 nSec non-cumulative jitter.

Without Pod (HP E1450 'Q' Inputs and Control Outputs)
Setup: 89 nSec
Hold: -71 nSec
Latency: 72 nSec to 88 nSec

With Pod (HP E1453 'Q' Inputs and Control Outputs)
Setup: 126 nSec
Hold: -103 nSec
Latency: 104 nSec to 125 nSec

End-if-ready Specifications

Function

The End-if-Ready (EIR) flag may be set in any Subcycle of any Timing Cycle (subject to the rules governing Timing Cycle length, Pattern Clock timing and Control Signal timing). When this flag is encountered and a Ready condition is indicated via external input(s), then that Timing Cycle will end after that Subcycle. If a Not Ready indication is given, the cycle continues past the EIR flag. With proper programming, this allows a DUT to request 'wait states' (up to the maximum defined length for that Timing Cycle) if it is not ready for the next cycle to begin. There is a TTL-compatible Ready coaxial connector (SMB-type) on the HP E1450 front panel and another on the HP E1453 Pod. These inputs have internal pull-ups, causing a default Ready indication if left open. Pulling either input low signifies Not Ready. The logic sense of these inputs can be programmatically inverted, and in this case, the unused input must be grounded before the other will be effective. For the front-panel coaxial connector, this is accomplished by attaching one SMB-type 50 Ω termination or short.

End-if-ready Specifications (cont'd)

'Ready' Input Levels And Loading

HP E1450A Front-Panel Coaxial Input

High:	> 2.0 V (internal pull-up)
Low:	< 0.8 V at < 250 uA
Capacitance:	< 10 pF, typical

HP E1453A Pod Input

High:	> 2.0 V (internal pull-up)
Low:	< 0.8 V at < 3.35 mA
Capacitance:	< 10 pF, typical

'Ready' Input Timing

The following definitions apply to an EIR flag which is set in a certain Subcycle:
Setup time is how long the specified 'Ready' input must be stable before the end of that Subcycle (as observed at the specified output) in order to ensure the desired operation. Hold time is how long the input must remain stable after the end of that Subcycle.

HP E1450 Front-Panel SMB Input/ HP E1450 'Control' Outputs

Setup:	72 nSec + 1 Subcycle
Hold:	–(58 nSec + 1 Subcycle)

HP E1450 Front-Panel SMB Input/ HP E1453 'Control' Outputs

Setup:	92 nSec + 1 Subcycle
Hold:	–(78 nSec + 1 Subcycle)

HP E1453 Input/ HP E1453A 'Control' Outputs

Setup:	104 nSec + 1 Subcycle
Hold:	–(89 nSec + 1 Subcycle)

Marker Specifications

Function

The Sequencer can be programmed to produce a Marker signal at any step of the Sequence. This Marker is available as both positive- and negative-going TTL/CMOS-compatible pulses via front-panel coaxial (SMB-type) connectors.It can also be programmatically directed to assert any or all of the VXI trigger busses.

Output Levels
Front-Panel SMBs

Maximum Continous Output Current:	± 24 mA
High, Open–Circuit:	> 4.4 V
Low, Open–Circuit:	< 0.1 V
Output Impedance:	~ 50 Ω
VXI Trigger Busses:	meet VXIbus specifications

Pulse Width

To Front-Panel SMBs:	Duration of Timing Cycle ± 5 nSec
To VXI TTL Trigger Bus:	Duration of Timing Cycle ± 5 nSec
To VXI ECL Trigger Bus:	≥ Two Subcycles ± 2 nSec

Miscellaneous Specifications

Power Requirements

+5 V (Excluding Control Output load current):
1.6A peak, 80 mA dynamic

–5.2 V:	8.9A peak, 150 mA dynamic
–2 V:	5.9A peak, 150 mA dynamic

Cooling Requirements

Average Power/Slot:	32 Watts
Ambient Temperature	
Operating:	0 to 55 °C
Storage:	–40 to 75 °C
Humidity:	65% relative from 0 to 40 °C
Airflow Required per Slot	
(for 10° rise):	.74 gal/sec at 0.04 Water (2.8 liter/sec at 0.9mm Water)
Weight:	6.61 lbs (3.0 kg)

HP E1451/E1452 I/O Pattern Modules and HP E1454 I/O Pod

Sequencer Specifications

Memory Depth 65,536 (64KB) vectors.
Multiple test sequences may co-reside in memory.

Memory Functions
Stimulus Pattern or Response Pattern (expected or recorded) as well as control of Tri-state, Compare, and End-of-Sequence functions.

Specifications For Ports Configured As Outputs

Clock Source
External Clock, HP E1450 Timing Module (one of six Stimulus Pattern Clocks)

Output Levels
HP E1451/E1452 Module Outputs

Maximum Continuous Output Current: ± 24 mA per line
High, Open-Circuit: 4.4 V, minimum
Low, Open-Circuit: 0.1 V, maximum
Output Impedance: 50 Ω, typical
Capacitance (outputs disabled): 30 pF, maximum
Leakage Current (outputs disabled): 20 uA, maximum

HP E1454 Pod Outputs

Maximum Continuous Output Current: ± 24 mA per line
High, Open-Circuit: 4.3 V, minimum
High, Sourcing 24 mA: 3.7 V, minimum
Low, Open-Circuit: 0.1 V, maximum
Low, Sinking 24 mA: 0.44 V, maximum
Capacitance (outputs disabled): 30 pF, maximum
Leakage Current (outputs disabled): 120 uA, maximum

Tri-State
Outputs can be disabled on a cycle-by-cycle basis by a control bit in the Sequencer memory, or by driving the Output Enable high. All eight pins of the port are controlled simultaneously.

Tri-State Control Input Levels and Loading
(for HP E1451/E1452 andHP E1454)
High: > 2.0 V at < 150 uA
Low: < 0.8 V (internal pull-down)

Tri-state Control Input Delay:
HP E1451/E1452 without pod:
9 nSec typical, 14 nSec maximum
HP E1454 with pod: 8 nSec typical, 11 nSec maximum

Timing
Pattern Rate: 0 to 20MHz
Skew:
Between output pins in the same port: 3 nSec, typical
Risetime: 6.5 nSec typical
Falltime: 7.0 nSec typical
Data Delay From External Clock:
HP E1451/E1452 without pod:
20 nSec typical, 27 nSec maximum
HP E1454 with pod: 14 nSec typical, 20 nSec maximum

Specifications For Ports Configured As Inputs

Clock Source
External Clock, HP E1450 Timing Module (1 of 6 Response Pattern Clocks)

Input Levels And Loading
(for HP E1451/E1452 and HP E1454):
Low: < 0.8 V at < 150 uA
High: > 2.0 V (internal pull-up)
Capacitance: 30 pF maximum

Real-time Compare
A programmable static mask can identify any pin of the port to be 'don't-care' for the duration of the test sequence. For those pins which are not masked, a Sequencer Control bit can enable the comparison of input patterns with expected response data on a cycle-by-cycle basis.

Input Timing
Setup Time to External Clock
HP E1451/E1452
without Pod: –1.6 nSec
HP E1454
with Pod: 5 nSec Hold Time from External Clock
HP E1451/E1452
without Pod: 11.5 nSec
HP E1454 with Pod: 14 nSec

External Clock Input Specifications
(for HP E1451/E1452 and HP E1454)

Minimum Period: 50 nSec
Minimum Pulse Width: 6 nSec
Polarity: Selectable
Input Levels (for HP E1451/E1452 or HP E1454):
Low: <0.8 V at <150 uA
High: >2.0 V (internal pull–up)
Capacitance: 30 pF maximum

Miscellaneous Specifications

Power Requirements
+5.0 V (excluding load currents): 1.5 A peak, 40 mA dynamic
–5.2 V: 2.2 A peak, 200 mA dynamic
–2.0 V: 0.6 A peak, 80 mA dynamic
+12.0 V: 0.1 A peak, 10 mA dynamic

Cooling Requirements
Average Power/Slot: 22W
Ambient Temperature:
Operating: 0 to 55°C
Storage: –40 to 75°C
Humidity: 65 % relative from 0 to 40°C
Operating temp: 0 to 55°C
Storage temp: –40 to 75°C
Airflow Requirements
(for 10° rise): .53 gal/sec at .05 Water
(2.0 liter/sec at 1.2 mm Water)

Weight: 2.43 lbs (1.1kg)

Configuring and Ordering the Model D20

Basic Structure

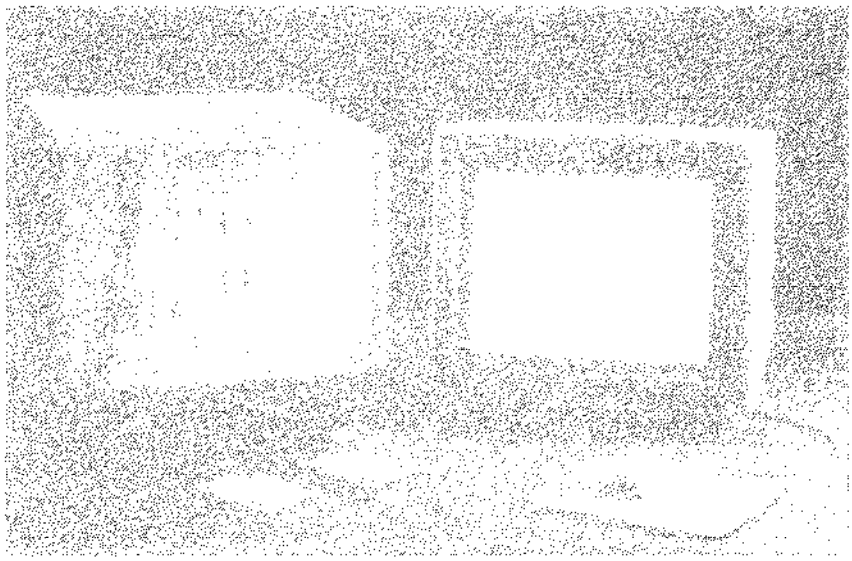
Downloadable SCPI Drivers: The HP E1405 System Firmware allows the downloading of drivers that support the use of SCPI commands with HP's register-based VXI modules. This firmware resides in the HP E1405 Command Module. The Model D20 requires downloaded drivers which are provided in the basic configurations listed below.

The HP 75000 Model D20 is structured for ordering in two basic configurations:

1 HP E1493A*: One HP E1450 Timing Module and HP E1453 Timing Pod, one HP E1452 Terminating Pattern I/O Module (32 I/O pins) with two HP E1454 Pattern I/O Pods, downloadable SCPI drivers in LIF and DOS formats (two 3.5-inch floppy disks) and documentation. SCPI drivers are for downloading the SCPI language into the HP E1405B (or E1405A with System Firmware Revision A.06 or later) Command Module. The HP E1400B Mainframe and E1405B Command Module are not included in the HP E1493A. The HP E1405 Command Module is required when the HP V/360 VXIbus embedded controller is used. The HP E1405 is also required for an HP-IB extended system as shown in Figure 14.

2 HP E1494A*: (same as 1 above plus HP E1496A Test Development Software.)

*VXIbus mainframe backplane connector shields are required in Europe for system compliance with RFI levels specified in standards EN55011 (European Norm) and CISPR11. Order HP E1400–80920 Backplane Connector Shield Kit, one per mainframe. This kit shields 13 slots (26 connectors).



HP 75000 Model D20 Digital Functional Test System

Expansion

Expansion of the basic configurations (HP E1493A or E1494A) described above is as follows (see Figure 17):

- First HP E1400B Mainframe with HP E1493A or E1494A:

  Opt.001—Adds one HP E1451A Pattern I/O Module (32 I/O pins) and two HP E1454 Pattern Pods). A maximum of six Opt.001s are permitted per E1400B Mainframe (Seven Pattern I/O Modules or 224 channels).

- Second and Third HP E1400B Mainframes (Figure 14):

  Configure the second and third HP E1400B mainframes as the first—with one E1493A and up to six Opt.001. In addition, one HP E1450–61603 Master/Slave Expansion Cable is required for each mainframe in the system. The HP E1405 Command Module is required in both the second and third mainframes when extended using HP-IB. If using the HP E1482A VXIbus Extender, the E1405 is only required in the first mainframe.

Wiring to the Model D20

When Using Pods

The pod mating connector (DUT side) is a 50-pin (2X25) male dual in-line connector such as the 3M 3596. These connectors are available from HP as P/N 1251–8832 (right angle) or 1251–8262. A pre-made cable is also available by ordering HP P/N E1493–61601. This cable is two feet long with color-coded, 26 gauge wires. One end is attached to a pod mating connector.

Wiring directly to the Module Front Panel

Cable assemblies for the front panels of the HP E1450A, E1451A, and E1452A can be purchased from HP. Both of these assemblies include the mating connector and a two foot, shielded cable with stripped and tinned ends:

- E1450A Timing Module: HP P/N E1453–61602
- E1451A/E1452A Pattern Modules: HP P/N E1454–61601

Otherwise, choose connectors from the 3M Mini D Cable family (50 pin).

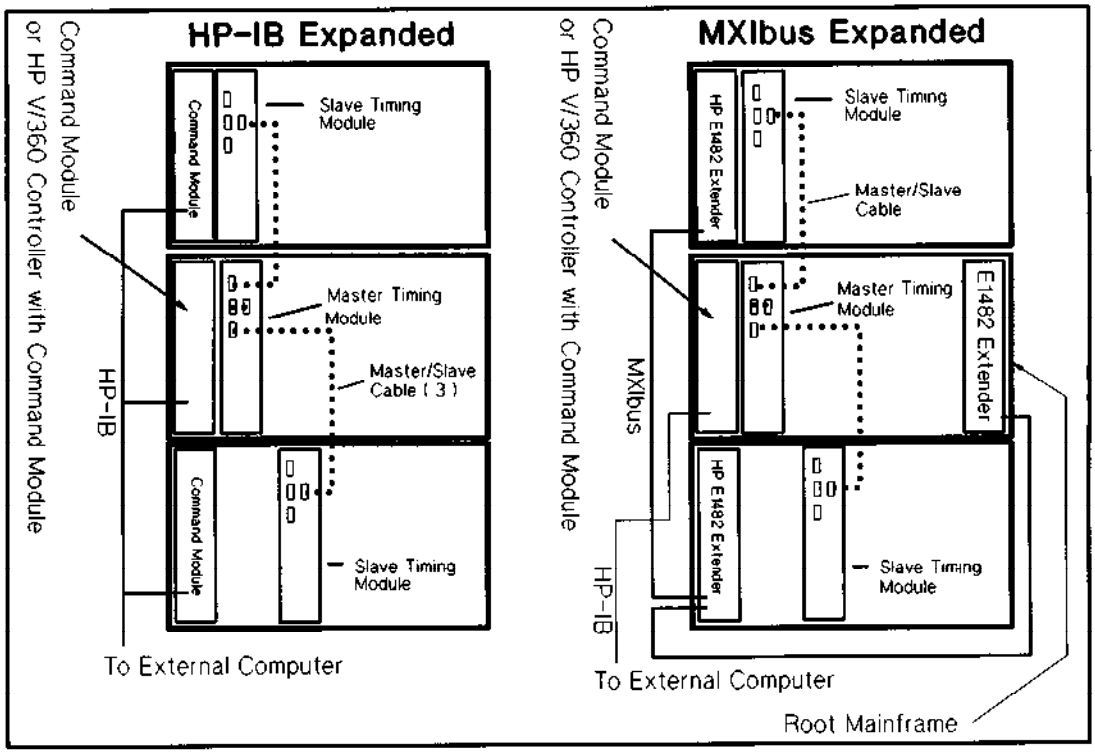


Figure 14. Multiple mainframe configurations using HP-IB or the MXIbus Extender (HP E1482).

Development Workstation Configuration (for HP E1496A)

The Development Software is supplied on a 1/4" tape cartridge. Requires an HP 9000 Series 300 or 400 HP-UX Workstation with:

- HP-UX 7.0, X/11, and OSF/Motif
- 8 Mbytes RAM minimum, 16 Mbytes recommended
- HP-IB (IEEE-488) interface, mouse
- Mid-range graphics (1024 x 768) or better, color recommended
- Workstation models recommended: HP 9000 Models V/360, 382, 380C+, 400s, or 425s.

NOTE:
MXIbus using the HP E1482A VXIbus Extender (Figure 14) requires HP E1405B firmware Rev A.08.

Product List
(All components listed below are orderable separately)

- HP E1400B: Series C Mainframe (module installation and rack accessory options listed in the HP VXIbus Catalog)
- HP E1405B: Command Module (memory and Instrument BASIC options listed in the HP VXIbus Catalog)

  Note: The HP E1400B and E1405B are available as a bundled product (HP E1492B) at a cost savings (see the HP VXIbus Catalog).
- HP E1450A: 160 MHz Timing Module
- HP E1451A: 20 MHz Pattern I/O Module
- HP E1452A: Terminating 20 MHz Pattern I/O Module
- HP E1453A: Timing Pod
- HP E1454A: Pattern Pod (two required per Pattern I/O Module)
- HP E1482A: VXIbus Extender (one per extended mainframe required)
- HP E1496A: Digital Test Development Software on 1/4-inch cartridge tape (SCPI drivers included)
- HP E1450–61603: Expansion Timing Module Master/Slave Cable (two required for second mainframe, one additional required for the third)
- HP E1450–80001: Downloadable SCPI Driver for Model D20 (Loads into the HP E1405B or E1405A with system firmware Rev A.06 or later)
- HP E1400–80920: Backplane Connector Shield Kit (one required per mainframe)
- HP E1405–80080: E1405A/B Firmware Update Kit (to Rev A.08). Allows SCPI driver Downloads and MXIbus support.

Model D20 Configuration Guide

Making sure you have all of the hardware components necessary to configure a Model D20 Digital Functional Test System requires calculating the number of Pattern I/O Modules. To determine the number needed, follow the simple four step process:

1 Determine the number of pins in each input and output groups required by your DUT. Bi-directional signals will require two groups: one input and one output.

2 Round up each group to the nearest multiple of eight (8). For example, 12 bi-directional data lines: 12 Input → 16 Input, 12 Output → 16 Output.

3 Divide each group by eight (8) to get the number of 8-pin ports. For example, 16/8=2 input ports, 16/8=2 output ports; the total number of input and output ports will determine the number of pattern I/O modules required (2+2=4 ports in this example), according to the accompanying chart.

4 The following configuration chart also provides mainframe, command module, and other hardware information required to configure the Model D20.

# Ports	E14008 [1] Quantity	E1405B [2] Quantity	E1493/E1494 [3] Quantity	E1450–61603 Expansion Cables Quantity	(3) Opt.001 Quantity
1–4					none
5–8					1
9–12					2
13–16	1	1	1 E1493 or E1494	none	3
17–20					4
21–24					5
25–28					6
29–32					6
33–36			1 E1493 or E1494	7	7
37–40			PLUS		8
41–44	2	2	1 E1493	2	9
45–48					10
49–52					11
53–56					12
57–60					12
61–64			1 E1493 or E1494		13
65–68			PLUS		14
69–72	3	3	2 E1493	3	15
73–76					16
77–80					17
81–84					18

1 One Shield Kit (E1450–80920) required for each mainframe for EMI compliance in Europe (EN55011).

2 Quantity indicated here is for a HP-IB extended system with external controller (Figure 14). For MXIbus expanded systems, one HP E1405B is required only for the root mainframe. In all configurations which use the HP E1405B, firmware Rev A.06 or greater is required.

3 Pattern I/O pods are included with Opt.001.

Glossary Of Terms

Condition ..... The current Boolean value of an Expression

Expression .... A combination of symbols representing Expression Input Pins (Q0, Q1,... Q9), and Boolean logic operators (AND, OR, etc.). The Boolean value of the Expression, i.e. its Condition, may be used to
1. validate triggers, or
2. establish test conditions.

Pattern ..... A pattern is an element of a vector. Patterns are the binary value on the pins of a pin group at a point in time. They are specified for each pin group assigned to a sequence. The binary patterns must contain the same number of bits as the number of pins in the pin group for which the pattern is specified.

Pattern Clock . A signal that contains one pulse during each timing cycle. It is used by pattern-type pin groups to advance to the next pattern in the sequence. There are two types of Pattern clocks: Stimulus and Response.

Pin Group ..... A named combination of pins (pins are the physical carrier for a signal). A pin group is physically limited to a combination of ports. Pin groups provide the physical interface between the sequence of patterns and the DUT. It is the defined 'pin-out' of the Model D20. More than one defined pin group can be assigned to a sequence to be able to generate more than one pattern in each vector. A sequence can contain more than one group of Stimulus patterns and more than one group of Response patterns.

'Q' Inputs ..... Inputs to the Timing Module that can be evaluated for validating triggers or establishing test conditions.

SCPI ..... Standard Commands for Programmable Instruments. SCPI commands are high level commands that initiate action by a programmable device. These commands cause specified functions to occur such as setting timing parameters, specifying pattern I/O channels, running a sequence, etc.

Sequence ..... A chronologically ordered set of Vectors containing pattern and timing cycle information.

Subcycle ..... A sub–element of a timing cycle. All events occur on subcycle boundaries; Timing Cycle Resolution equals the duration of each subcycle.

Timing Cycle .. A timing cycle is the length of time a vector is active and is made up of a number of subcycles. Each timing cycle can be a different number of subcycles long, and can have various events (such as pattern clocks) occur at different times.

Trigger Event . An event which satisfies the Wait-for-Trigger state of the trigger mechanism and causes a transition to the Wait-for-Arm state.

Trigger Qualifier ..... A condition (Cond 3) which, when true, allows a transition on the selected trigger input to be seen as a Trigger Event.

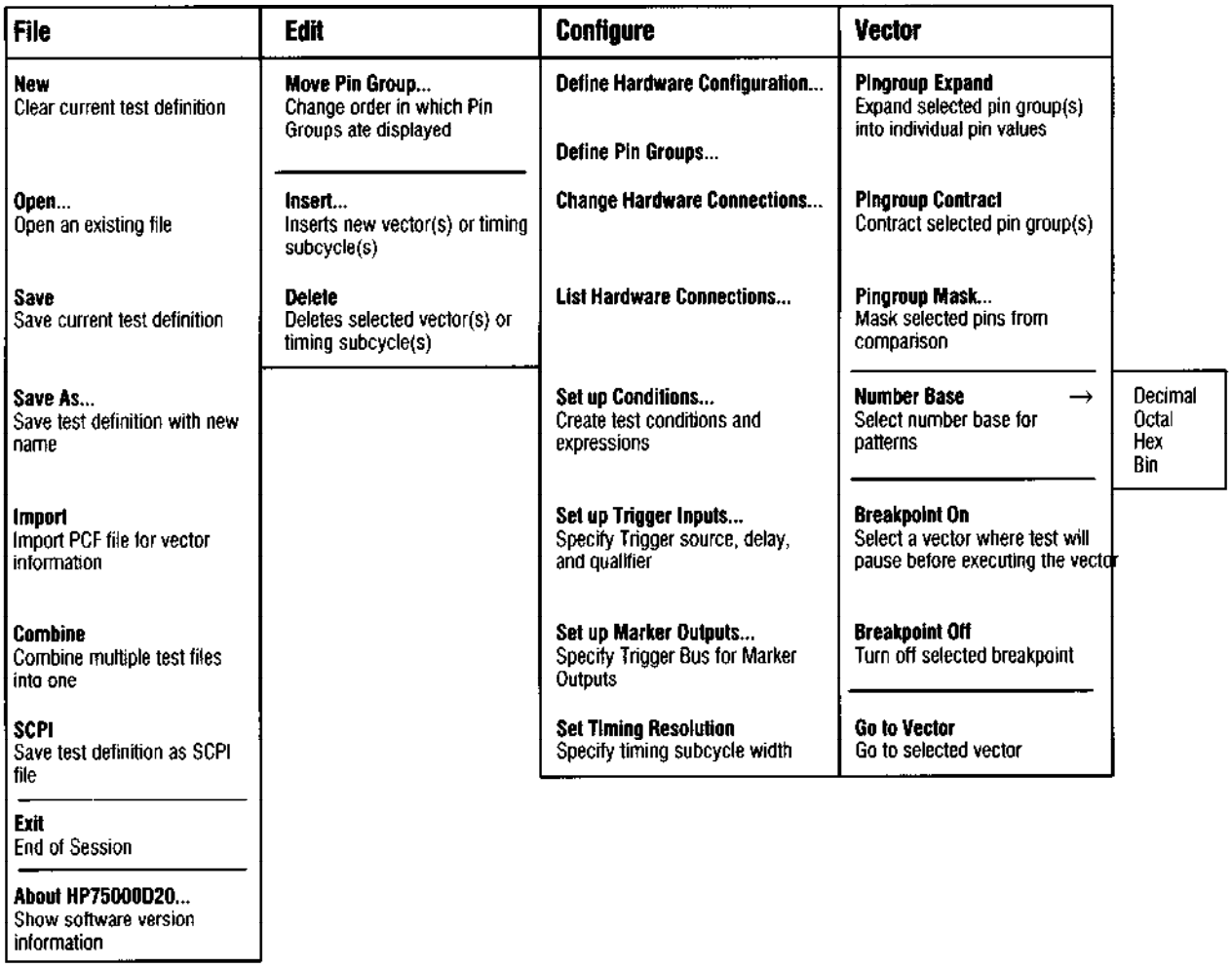
Tri–state ..... The 'Off' or high-impedance state of a stimulus pin group. When two pin groups are connected together for bi-directional operation, the stimulus pin group must be tri-stated while the response pin group is receiving patterns.

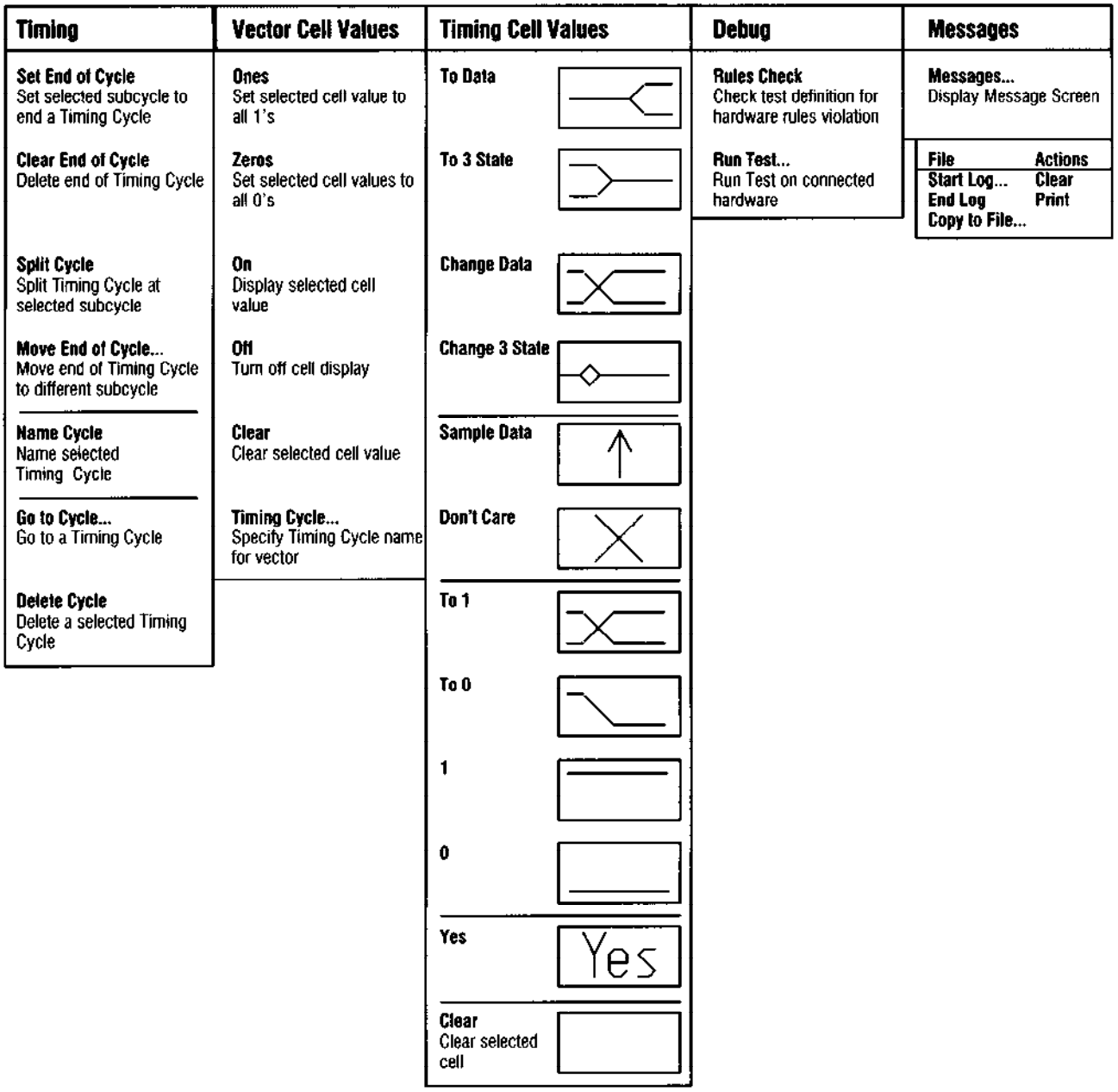
Vector ..... A vector is the set of information that defines one step of the sequence. A vector contains the following information: pattern data for each pin group, the name of the timing cycle which is to be used for that step, whether to arm the trigger, and whether to generate a marker pulse.

Wait-for-Trigger State ..... The trigger mechanism has been armed and the instrument is Trigger State waiting for the specified trigger event to occur. When the trigger event occurs, the instrument will resume operation.

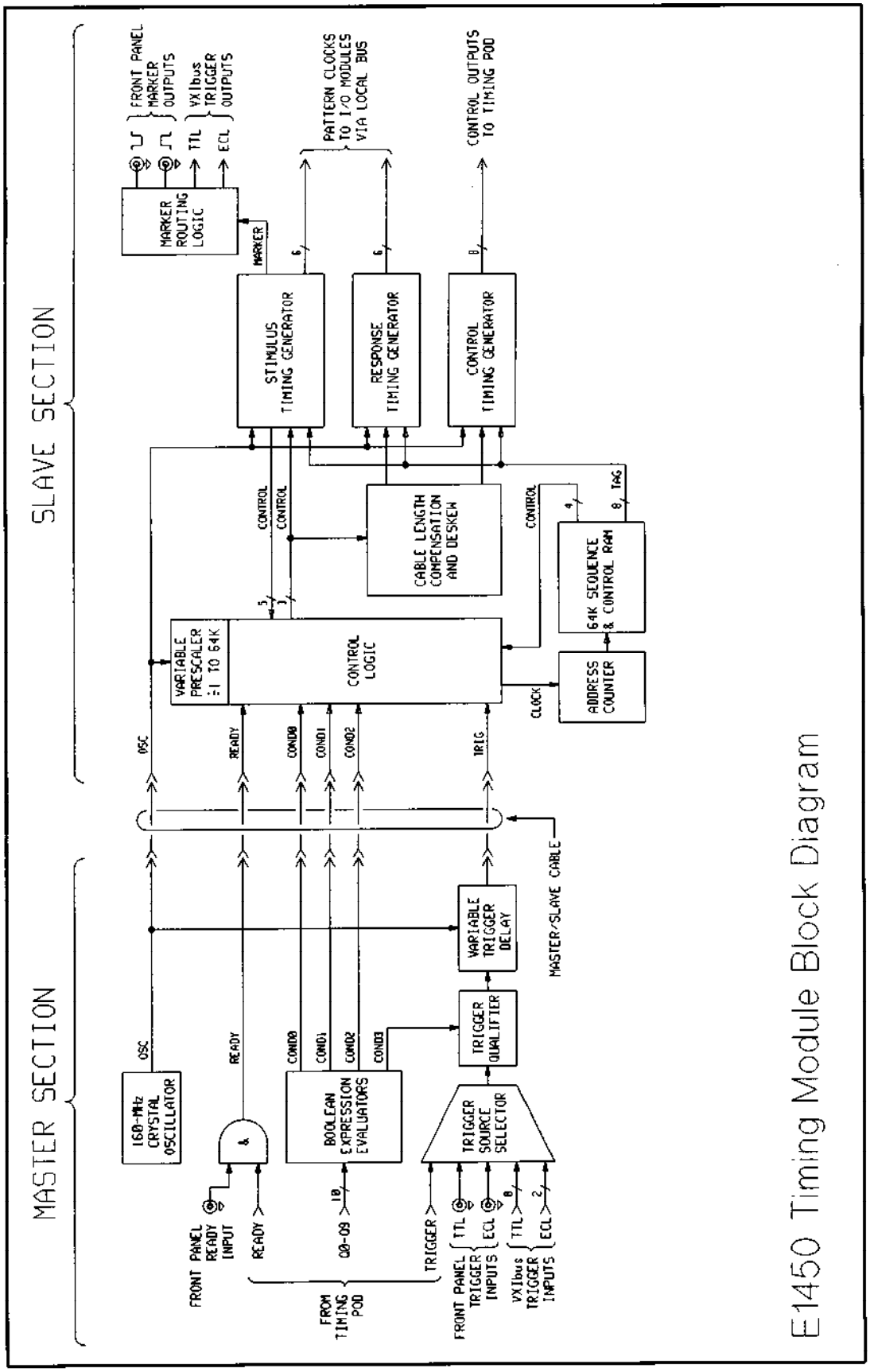
Wait-for-Conditions State ..... The System has encountered an 'Await Condition' in the timing Conditions cycle and the specified condition is false, causing all State activity to stop. Operation will resume when the condition becomes true.

Appendix I – Pull-down Menus

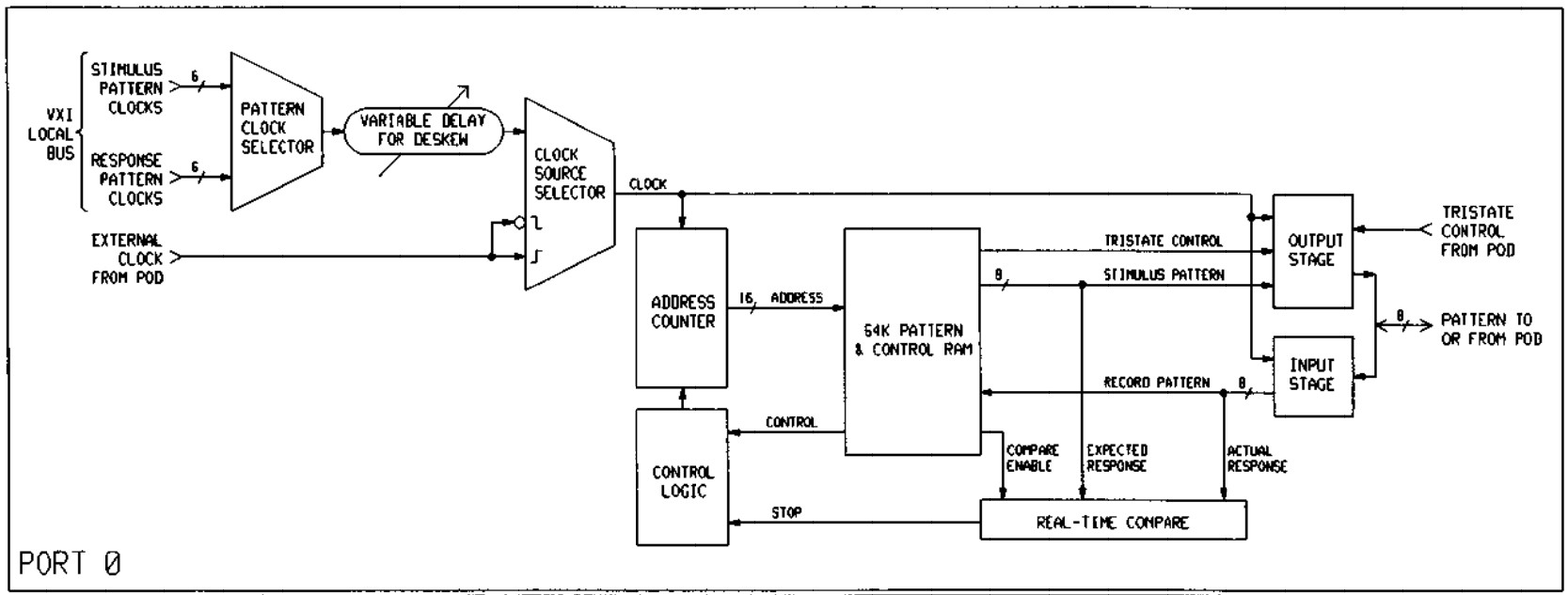



Timing
Set End of Cycle
Set selected subcycle to end a Timing Cycle
Clear End of Cycle
Delete end of Timing Cycle
Split Cycle
Split Timing Cycle at selected subcycle
Move End of Cycle...
Move end of Timing Cycle to different subcycle
Name Cycle
Name selected Timing Cycle
Go to Cycle...
Go to a Timing Cycle
Delete Cycle
Delete a selected Timing Cycle
Vector Cell Values
Ones
Set selected cell value to all 1's
Zeros
Set selected cell values to all 0's
On
Display selected cell value
Off
Turn off cell display
Clear
Clear selected cell value
Timing Cycle...
Specify Timing Cycle name for vector
Timing Cell Values
To Data
To 3 State
Change Data
Change 3 State
Sample Data
Don't Care
To 1
To 0
1
0
Yes
Yes
Clear
Clear selected cell
Debug
Rules Check
Check test definition for hardware rules violation
Run Test...
Run Test on connected hardware
Messages
Messages...
Display Message Screen
File
Actions
Start Log...
Clear
End Log
Print
Copy to File...

Appendix II – Block Diagrams



HP E1450 Timing Module Block Diagram



E1451/1452 Pattern I/O Module Block Diagram

HP E1451/1452 Pattern I/O Module Block Diagram

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